DIGITAL DELAYING DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a signal delay device, and more particularly to a digital delaying device.

Description of the Related Art

There are various formats in the data write control specifications for an optical disc such as CD-R, CD-RW, DVD, and the like. The formats, which allow writers to write multilevel data to the optical disc, are sequentially proposed. Therefore, it is more important to precisely control the laser waveform for writing data to the optical disc.

FIG. 1 shows a schematic illustration of a laser write waveform of a CD-R. As shown in FIG. 1, the laser write waveform is a write power from time t0. The write power is held until time t1 and is dropped to an erase power, which is held until time t2. Next, the laser write waveform is again dropped to a read power. The length from time t1 to time t2 is determined by the mark length to be written. The length from time t0 to time t1 is program-controlled and does not vary with the change of the mark length. The basic unit of the mark length is T, and the mark length ranges form 3T to 11T in the CD-R specification. In addition, the leading edge of the laser write waveform at time t0 has about a delay length Δt, which is substantially equal to 0.25T. The delay length Δt is

only needed when the previous write mark is 3T. Consequently, it is quite important to precisely control the switch timing of the laser write waveform.

U.S. Patent No. 6,269,060, entitled "Programmable write signal generator" has disclosed a technology for generating a write signal. FIG. 2 shows a block diagram of the delay signal generating unit of this patent. Referring to FIG. 2, the delay signal generating unit 506 includes an upper course delay unit and a lower fine delay unit. The output signal of the course delay unit is supplied to the fine delay unit, which may precisely control the delay timing. As shown in the drawing, the delay timing of the course delay unit is 2.5ns while the delay timing of the fine delay unit is 0.25ns. Each delay unit includes a plurality of cascaded delay cells D1(D2), a multiplexer 612(632), and a selection signal generator 610(630). The plurality of cascaded delay cells D1(D2) receives the input signal, and then a plurality of signals with different delay timings are generated. Next, the multiplexer 612(632) selects one of the signals for output according to a selection signal, which is supplied from the selection signal generator 610(630). Because the patent utilizes voltage control delay cells in the delay lock loop (DLL), it discloses an analog control method, and the charge pumps in the DLL are also of an analog design. In general, the analog design is more complicated and tends to be influenced by the environment.

SUMMARY OF THE INVENTION

In view of the above-mentioned problems, an object of the invention is to provide a digital delaying device, which precisely controlling the delay timing of the input signal.

To achieve the above-mentioned object, the invention provides a digital delaying device for delaying an input signal using digital method. The digital delaying device includes a ring oscillator, a calibration unit, and at least one delay number calculation unit and delay channel. The ring oscillator includes loop-connected delay cells for outputting an oscillation clock. The calibration unit receives a reference clock and the oscillation clock and calculates a pulse number of the oscillation clock corresponding to each reference clock period. The pulse number serves as a period reference pulse number. The calculation unit receives the pulse number and a signal delay value, calculates a signal delay number corresponding to the signal delay value according to the pulse number, and outputs a selection signal. The delay channel includes a multiplexer and cascaded delay cells, which receives an input signal and generates delay signals with different delay timings. The multiplexer selects and outputs one of the delay signals as an output signal according to the selection signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic illustration of a laser write waveform of a CD-R.

FIG. 2 shows a block diagram of a conventional delay signal generating unit.

FIG. 3 shows a block diagram of a digital delaying device according to a first embodiment of the present invention.

FIG. 4 shows a block diagram of a ring oscillator of the first embodiment.

FIG. 5 shows a block diagram of a calibration unit of the first embodiment.

FIG. 6 shows a block diagram of a delay channel of the first embodiment.

FIG. 7 shows a block diagram of a digital delaying device according to a second embodiment of the invention.

FIG. 8 shows a block diagram of a digital delaying device according to a third embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The digital delaying device using digital method of the invention for delaying a signal will be described with reference to the accompanying drawings.

FIG. 3 shows a block diagram of a digital delaying device according to a first embodiment of the invention. The digital delaying device 30 of the invention for delaying a signal includes a ring oscillator 31, a calibration unit 32, a delay number calculation unit 33, and a delay channel 34. The digital delaying device (signal delay device) 30 of the invention utilizes the ring oscillator 31 to generate an oscillation clock and utilizes the calibration unit 32 to correct a pulse number of the oscillation clock, which corresponds to each reference clock period and serves as a period reference pulse number C. Then, the delay number calculation unit 33 receives a signal delay value m and calculates a delay pulse number Dn corresponding to the signal delay value m according to the period reference pulse number C. Finally, the signal delay device 30 utilizes the delay channel 34 to delay an input signal by a desired period of time according to the delay pulse number Dn and then outputs an output signal.

FIG. 4 shows a block diagram of a ring oscillator of the first embodiment.

Referring to FIG. 4, the ring oscillator 31 includes a plurality of delay cells 311 to 31N connected in a loop, and an NAND gate (or NOR gate) 310. The cascaded delay cells 311 to 31N form a close loop via the NAND gate 310, and receive a reset signal for resetting the ring oscillator 31. The ring oscillator 31 outputs an oscillation clock having a period (frequency) determined by the delay timing of the delay cells and the number of the delay cells. The period of the reference clock may be equal to the basic unit T of the mark length of the optical disc.

The period of the oscillation clock may vary with the variation of the wafer foundry, chip, operation voltage, and operation environment. Therefore, the invention utilizes the calibration unit to calibrate the period of the oscillation clock with a stable reference clock and to output a period reference pulse number C as a reference standard for delay. FIG. 5 shows a block diagram of a calibration unit of the first embodiment. Referring to FIG. 5, the calibration unit 32 includes two frequency dividers 321 and 322, a rising edge pulse generator 323, a counter 324, and a register 325. The calibration unit 32 calculates a pulse number of the oscillation clock corresponding to each reference clock period and outputs the pulse number as a period reference pulse number C. The frequency dividers 321 and 322 receive the reference clock and the oscillation clock, divide them by the same value, and then output frequency-divided clocks S1 and S0, respectively. The rising edge pulse generator 323 receives the frequency-divided clock S1 and generates a pulse on a pulse signal S2 at each rising edge of the frequency-divided clock S1. The counter 324 counts the pulse number of the pulse signal S2 and the pulse signal S2 serves as a clear signal. The register 325

stores the count value of the counter 324 before it is cleared, and the stored value serves as the period reference pulse number C. The function of the frequency dividers 321 and 322 is to reduce the frequencies of the reference clock and the oscillation clock and make the counter 324 count easily. If the frequencies of the oscillation clock and the reference clock are not too high, the frequency dividers 321 and 322 may be omitted. The frequency-divided values of the frequency dividers 321 and 322 may be the same or different. If the frequency-divided values of the frequency dividers 321 and 322 is different and the frequency-divided values of 322 is "A" times that of 321, the reference pulse number C may be multiplied by "A," or "A" may be output to the delay number calculation unit 33 for further processing as described latter. Before the reference pulse number C is output, it may pass a low-pass filter (LPF) to ease the variation of the reference pulse number C when the reference period changes.

The delay number calculation unit 33 receives a signal delay value and the period reference pulse number C and calculates a representative delay number of the signal delay value to serve as a selection signal. The representative delay number means the pulse number of the oscillation clock to be delayed. The calculation function for the delay number calculation unit 33 is:

$$F(m,M,C)= (m/M) * C \qquad (1),$$

wherein M represents the number of minimum delay units contained in the reference clock period, m represents the signal delay value (i.e., the number of the minimum delay units to be delayed by the signal), and C represents the pulse number of the period reference. For example, when C is 32, M is 16, and the

signal delay value m is 2, which means the delay number is (2/16) that of the reference clock period, the selection signal is equal to 4 according to the calculation result of Equation (1). If the frequency-divided values of the frequency dividers 321 and 322 are different and the frequency-divided values of the frequency dividers 322 is "A" times that of the frequency dividers 321, the calculation function for the delay number calculation unit 33 is:

$$F(m,M,C,A) = (m/M) * C * A \qquad (2).$$

FIG. 6 shows a block diagram of a delay channel of the first embodiment. Referring to FIG. 6, the delay channel 34 includes P cascaded delay cells 341 to 34P, and a multiplexer 340. The P cascaded delay cells 341 to 34P receive an input signal and generate P delay signals with different delay timings, and output the P delay signals along with the input signal to the multiplexer 340. The multiplexer 340 outputs one of the delay signals as the output signal according to the selection signal. That is, when the selection signal is 0, the input signal is selected and output. When the selection signal is 1, the output signal of the first delay cell 341 is selected and output, and so on. Since the delay cells 341 to 34P of the delay channel 34 and the delay cells 311 to 31N of the ring oscillator 31 have the same design, the delay timing of each of the delay cells 341 to 34P and that of each of the delay cells 311 to 31N are the same.

According to the architecture of the invention, the digital delaying device of the invention for delaying a signal utilizes a ring oscillator to generate an oscillation clock and a calibration unit to calculate a period reference pulse number. Then, the delay number calculation unit calculates the delay number of

the input signal. Next, a delay channel is utilized to generate an output signal with correct delay timing. Since the delay cells of the delay channel and the ring oscillator are manufactured in the same manufacturing process, the delay timings of the delay cells of the ring oscillator and the delay channel are the same and never change with the variations of the environment or manufacturing processes.

FIG. 7 shows a block diagram of a digital delaying device according to a second embodiment of the invention. The digital delaying device 30 of the first embodiment only includes a set of the delay number calculation unit 33 and the delay channel 34, while the digital delaying device 30' of the second embodiment includes N sets of delay number calculation units 33 and delay channels 34. Therefore, the digital delaying device 30' may simultaneously provide N sets of output signals with different delay timings.

FIG. 8 shows a block diagram of a digital delaying device according to a third embodiment of the invention. In the digital delaying device 30 of the first embodiment, it is assumed that the calculating time for the delay number calculation unit 33 is smaller than a minimum delay number. So, the input signal is directly input to the delay channel. In this case, no output timing delay of the output signal will be caused even though the signal delay value m is 1. In contrast, the digital delaying device of the third embodiment of FIG. 8 utilizes the calculating time, which is greater than the minimum delay number, for the delay number calculation unit 33. In order to avoid the output timing delay of the output signal, a flip-flop set 35 is employed to output the selection signal and the input signal synchronously. The flip-flop set 35 synchronously outputs the

selection signal and the input signal according to a reference clock serving as a trigger signal.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific construction and arrangement shown and described, since various other modifications may occur to those ordinarily skilled in the art.